IN THE SPECIFICATION:

Please amend the specification as follows:

(1) The paragraph from page 2, line 16 to page 2, line 30 has been amended as follows:

Figure 1 illustrates an example of general structure of SoC 10 that has an embedded memory 12, a microprocessor core 14, and three function-specific cores 16, 18 and 20, PLL (phase lock loop) 22 and TAP (test access port) 24. The overall testing of SoC can be done only through the chip-level I/Os. In this example, such chip level I/Os are established as chip I/O pads 28 formed on ~~a~~ an I/O pad frame 26 at the outer periphery of SoC 10. Each of the functional cores 12, 14, 16, 18 and 20 includes a pad frame 29 which is typically contains multiple I/O pads of cores at core periphery. Generally, in IC design, the top metal layer is used for only power pads 32 for power sources while intermediate metal layers are used for I/O or signal pads for interfacing with other cores, microprocessor core and embedded memory.

(2) The paragraph from page 7, line 12 to page 7, line 20 has been amended as follows:

Referring now to Figures 3 and 4, there is shown a basic concept in the present invention to establish an I/O interface for each core that can be directly accessible by traditional contact probes. In the present invention, the I/O interface of an individual core can be used for test signal application

and response signal observation. Consequently, it is able to apply a core test pattern (rather than a chip test pattern) directly to a particular core, i.e., it is only necessary to access the I/Os of the core.

(3) The paragraph from page 7, line 30 to page 8, line 2 has been amended as follows:

In the present invention, however, for a manufacturing process that supports plural layers of metal, an I/O pad-frame of each core is duplicated upwardly for all of the metal layers to the top layer. As shown in Figure 3, I/Os of each core are brought-up to the top-level metal of the SoC without using any logic or complex sense structure. Thus, the I/O pad-frame of each core can be accessed by contact probes without any intervention. For simplicity of illustration, I/O pads at the top-level metal are omitted.